Remarks

Claims 1-4 and 7-11 are pending in the subject application and currently stand rejected. Reconsideration and favorable consideration of the pending claims is respectfully requested in view of the following remarks.

Claims 1-4 and 7-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Scott (U.S. Patent 6,627,524) in view of Pradeep *et al.* (U.S. Patent 5,866,448) or Zhou *et al.* (U.S. Patent 5,858,847). Applicant respectfully traverses, noting that a *prima facie* case of obviousness has not been presented. Three criteria must be met to establish *prima facie* case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the prior art reference, or combination of references, must teach or suggest all the claim limitations.

Scott teaches, at col. 2, lines 11-24,

> "a method of forming at least two programmable read-only memory constructions. At least one conductive material is formed over a semiconductor substrate. At least two patterned photoresist blocks are formed over the conductive material, with a pair of adjacent photoresist blocks being separated by a first gap. A coating is formed over the pair of adjacent photoresist blocks and across the first gap between the adjacent blocks. The coating is selectively removed from across the first gap while leaving the coating on the pair of adjacent photoresist blocks. The pair of photoresist blocks and coating remaining on the pair of photoresist blocks together define a pair of masking blocs that are separated by a second gap. The second gap is narrower than the first gap. A pattern is transferred from the masking blocks to the conductive material to pattern a pair of spaced floating gate constructions from the conductive material."

Accordingly, as the Office Action at page 2 admits, Scott fails to disclose patterning the sacrificial layer to form polymer layers on sidewalls of the sacrificial layer, the polymer layers being generated from the etching of the sacrificial layer, wherein the polymer layers on the sidewalls of the sacrificial layer are separated by less than a lithographic minimum feature size as claimed in claims 7 and 10 of the subject application. Rather, Scott forms a photoresist layer on a conductive material (such as polysilicon), patterns the photoresist layer in order to create photoresist blocks, forms a coating over the photoresist blocks and then selectively removes the coating that is not cross-linked with the photoresist. Regarding the cross-linking, Scott teaches, at col. 4, lines 15-22 "The crosslinking can bond the coating to blocks 18 and 20 and/or form the coating into a shell tightly adhered with blocks

18 and 20. The material designated as AZ R200™ is but one material which can be utilized in methodology of the present invention . . . Other materials which selectively bond or adhere to photoresist blocks 18 and 20 can be used alternatively to the material designated as AZ R200™."

The Office Action at page 3 states that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Scott so as to form the polymer layers by etching the sacrificial layer because this would reduce the overall number of process steps, thereby decreasing process time." However, replacing the three steps in Scott of patterning the photoresist layer, forming a coating over the photoresist blocks, and selectively removing the coating with the steps in subject claim 1 of patterning the sacrificial layer to form polymer layers on sidewalls of the sacrificial layer, the polymer layers being generated from the etching of the sacrificial layer, does not reduce the overall number of process steps. Indeed, an embodiment of patterning the sacrificial layer to form polymer layers on sidewalls of the sacrificial layer is described in the subject application, at paragraphs [0009]-[0010], as where "Referring to Fig. 2c, a photoresist pattern 41 is formed on the first sacrificial layer 39 . . . Referring to Fig. 2d, an etching process is performed using the photoresist pattern 41. At the same time, polymers generated from the etching of the first sacrificial layer 39 are attached to the sidewalls of the etched first sacrificial layer 39 to form polymer layers 43." Accordingly, patterning the sacrificial layer to form polymer layers on sidewalls of the sacrificial layer can incorporate the three steps of forming a photoresist layer, patterning the photoresist, and etching the sacrificial layer. Therefore, there is no motivation to modify the process of Scott to maintain the same number of process steps.

In addition, as described above, Scott uses a material that can selectively bond or adhere to the photoresist and as such does not require a material that generates polymers from its etching in order to form a floating gate and tunnel oxide using the newly formed blocks as masks. Therefore, a person of ordinary skill in the art at the time the invention was made would not have been motivated to modify Scott to arrive at the subject method as claimed in any of claims 1-4 and 7-11.

Moreover, Pradeep *et al.* and Zhou *et al.* do not cure this defect. Pradeep *et al.* discloses a process for forming a lightly doped-drain (LDD) structure where the forming of a polymer sidewall provides the advantage, as described at col. 3, lines 34-36, "that the sidewall oxide deposition onto the silicon active area is eliminated, thereby reducing the risk of channel contamination." This sidewall oxide deposition described in Pradeep *et al.* is **not** present as a problem in Scott. Therefore, Pradeep *et al.* does not provide any motivation to modify Scott. Zhou *et al.* also discloses a process

for forming a LDD structure. Zhou *et al.* describes the need to provide, as stated at col. 3, lines 28-33, "a simpler method of forming the lightly doped drain structure that eliminates the process steps of spacer oxide deposition and spacer etch . . . [t]he width of the polymer layer and the lightly doped drain is highly controllable and can be formed thinner than traditional dielectric and photoresist spacers." Again, spacer oxide deposition and etch are **not** present as a problem in Scott. Therefore, Zhou *et al.* does not provide motivation to modify Scott. The law is clear that using one's application as a guide for hindsight reconstruction of the invention is improper. Combining steps from various references to modify them merely because they can be combined is not enough. To provide a *prima facie* case of obviousness, one must find the motivation to modify the teachings in the prior art, not in Applicant's specification. Scott does not drive the ordinary artisan to seek modification, and neither Pradeep *et al.* nor Zhou *et al.* provide motivation to modify Scott to arrive at the subject invention as claimed.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-4 and 7-11 under 35 U.S.C. § 103(a).

In view of the foregoing, Applicant believes that the currently pending claims are in condition for allowance, and such action is respectfully requested.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

The applicant invites the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

Jeff Lloyd
Patent Attorney
Registration No. 35,589
Phone No.: 352-375-8100
Fax No.: 352-372-5800
Address: Saliwanchik, Lloyd & Saliwanchik
A Professional Association
P.O. Box 142950
Gainesville, FL 32614-2950

JL/gyl/sjk/amh
Attachments: Request for Continued Examination including Petition and Fee for Extension of Time.